

# SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE

## BACKGROUND OF THE INVENTION

The present invention relates to a semiconductor integrated circuit device and more specifically to the technology which can effectively be applied to a voltage step-down power supply circuit, for example, of one-chip microcomputer.

Following documents have been reported as the prior arts of a semiconductor integrated circuit device including an internal voltage step-down power supply circuit. The Japanese Published Unexamined Patent Application No. 117650/2001 (hereinafter referred to as the prior art 1) describes that power consumption in the standby operation can be lowered by using an internal voltage step-down circuit for active condition, for the active operation, which shows large current consumption but assures excellent response characteristic and an internal voltage step-down circuit for standby condition, for the standby operation, which is inferior in the response characteristic but shows small current consumption through the switching operation. The document, "A tunable CMOS-DRAM Voltage Limiter with Stabilized Feedback Amplifier", IEEE J.SOLID-STATE CIRCUITS, Vol. 25, No. 5, OCT.1990 (hereinafter referred to as the document 2) describes voltage trimming through the switching of the

serial/parallel conditions of MOSFET.

[Patent Document 1]

Japanese Published Unexamined Patent Application No.  
117650/2001

[Non-Patent Document 1]

"A tunable CMOS-DRAM Voltage Limiter with  
Stabilized Feedback Amplifier", JEEE J. SOLID-STATE  
CIRCUIT, Vol. 25, No. 5, OCT. 1990

#### SUMMARY OF THE INVENTION

The inventors of the present invention have discussed reduction of standby current in a semiconductor integrated circuit device mounted in a CPU (microprocessor) up to about 1  $\mu$ A. As a result, the inventors have found that a high resistance must be used in order to realize low power consumption as described above in the voltage step-down power supply circuit for standby use like the prior art 1, and also have encountered a problem that when such high resistance is formed on a semiconductor substrate, a resistance element requires a huge installation area. Therefore, it has been attempted to form a voltage step-down power supply circuit using the circuit including the MOSFET described in the prior art 2 but it is also proved that this circuit structure has a problem that temperature characteristic is left unsolved when voltage is adjusted with the trimming or

the like and thereby the accuracy is lowered.

Moreover, in the semiconductor integrated circuit device such as the conventional DRAM in which a standby current as high as 100  $\mu$ A or more flows, it is assumed that a particular problem does not occur. However, in the device having various circuit functions such as a system LSI where the CPU and its peripheral circuits are mounted to only one semiconductor integrated circuit device, it has been proved that when the structure where the reference power supply circuit for active condition is stopped to reduce the current in the standby operation is formed, the reference power supply circuit for active condition must be re-started when the standby condition is switched to the active condition, a longer time is required until the internal voltage reaches the predetermined stable voltage condition, an error is generated in the operation when the internal circuit such as the CPU is operated simultaneously with the switching to the active condition, or particular attention must be paid to operation of the voltage step-down power supply circuit in order to realize automatic trimming of the voltage step-down by the CPU.

It is an object of the present invention to provide a semiconductor integrated circuit device including a voltage step-down power supply circuit which has realized high performance and low power consumption even when the installation area is reduced. Another object

of the present invention is to provide a semiconductor integrated circuit device which has realized automatic voltage adjustment of two voltage step-down power supply circuits for active condition and standby condition. The aforementioned and the other objects and novel features of the present invention will become apparent from the description of the present specification and the accompanying drawings thereof.

The typical inventions of the invention disclosed in the present specification are briefly summarized as follows. A first reference voltage is formed by amplifying a fixed voltage generated with a fixed voltage generating circuit with an amplifying circuit of which voltage gain is adjusted with a resistance circuit and a switch controlled with a first trimming switch setting signal, a first output buffer which is activated with a first control signal outputs an internal step-down voltage when the internal circuit is in the active condition, a second reference voltage is formed by adjusting the combination of the threshold value voltages of the MOSFETs with a plurality of MOSFETs and a switch controlled with a second trimming switch setting signal, and an internal voltage step-down in the standby condition of an internal circuit is outputted from a second output buffer which is activated with a second control signal.

## BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a block diagram showing an embodiment of a microcomputer LSI to which the present invention is applied.

Fig. 2 is a block diagram showing an embodiment of a power supply circuit VG of Fig. 1.

Fig. 3 is a block diagram showing another embodiment of the power supply circuit VG of Fig. 1.

Fig. 4 is a waveform diagram for describing an example of operations of the power supply circuit in relation to the present invention.

Fig. 5 is a waveform diagram for describing an example of operations of a READYREG signal generating circuit of Fig. 3.

Fig. 6 is a block diagram showing another embodiment of the power supply circuit VG of Fig. 1.

Fig. 7 is a practical circuit diagram showing an embodiment of a reference voltage 2 generating circuit of Fig. 2.

Fig. 8 is a practical circuit showing another embodiment of the reference voltage 2 generating circuit of Fig. 2.

Fig. 9 is a temperature characteristic diagram for describing operations of the reference voltage 2 generating circuit of Fig. 8.

Fig. 10 is a circuit diagram showing another embodiment of a voltage step-down power supply circuit

for active condition in relation to the present invention.

Fig. 11 is a circuit diagram showing another embodiment of the READYREG signal generating circuit provided in the voltage step-down power supply circuit for active condition in relation to the present invention.

Fig. 12 is a block diagram showing another embodiment of the power supply circuit VG of Fig. 1.

Fig. 13 is a circuit diagram showing another embodiment of the READYREG signal generating circuit provided in the voltage step-down power supply circuit for active condition in relation to the present invention.

#### DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Fig. 1 is a block diagram of an embodiment of a microcomputer LSI to which the present invention is applied. Each circuit block of this figure is formed on single substrate such as a single crystal silicon substrate with the well known CMOS (complementary MOS) semiconductor integrated circuit manufacturing technology.

The microcomputer LSI described above is intended, although not particularly restricted, to application into mobile devices which have realized high performance arithmetic processes and integrated peripheral units

required for system configuration by introducing a RISC (Reduced instruction set computer) type central processing unit CPU. The CPU has a RISC type instruction set and the basic instruction operates on the one instruction and one state (one system clock cycle) basis through the pipeline process. Following peripheral circuits are also mounted around the CPU and data signal processor DSP, for example, to form a mobile telephone.

An internal bus is composed of I bus, Y bus, X bus, L bus and peripheral bus and a memory XYMEM and a memory controller XYCNT for image process are also provided as the built-in peripheral modules to form a user system with the minimum number of components. These memory XYMEM and controller XYCNT are connected to the I bus, X, Y buses and L bus and the data output operation is executed for data input/output and display operation for image process.

The I bus described above is provided with a cache memory CACHE, a cache memory controller CCN, a memory management controller MMU, a translation look-aside buffer TLB, an interruption controller INTC, a clock oscillator/ watch-dog timer CPG/WDT, a video I/O module VIO and an external bus interface. These are connected to an external memory LSI or the like not illustrated via this external bus interface.

The L bus is connected to the cache memory CACHE,

cache memory controller CCM, memory management controller MMU and translation look-aside buffer TLB described above, a central processing unit CPU, a data signal processor DSP, a user break controller UBC and an advanced user debugger AUD.

The peripheral bus described above is connected to a timer unit TMU of 16 bits, a compare match timer CMT, a serial I/O (with FIFO) SIOF0, a serial communication interface SCIF1 with built-in FIFO, a I<sup>2</sup>C controller I<sup>2</sup>C, a multi-function interface MFI, a NAND/AND flash interface FLCTL, a user debug interface H-UDI, an ASE memory ASERAM, a pin function controller PFC, a RCLK operation watch dog timer RWDT. The peripheral bus and I bus described above are also connected with a bus state controller BSC and a direct memory access controller DMAC.

The power supply circuit VG receives a comparatively higher external voltage as high as 3.0V, for example, supplied from an external terminal, forms a step-down voltage as low as 1.4V to 1.6V when the internal circuit of the CPU or the like is in the active condition, and also forms a step-down voltage as low as 1.3 to 1.7V when the internal circuit of the CPU or the like is in the standby condition. Such step-down voltages are supplied as the operation voltages to each interval circuit as described above. However, the external bus interface includes an input circuit, an



output circuit and a level converting circuit for sending and receiving signal level corresponding to the external voltage of about 3V and these input circuit, output circuit and level converting circuit are fed with an external voltage in place of the step-down voltages described above.

Fig. 2 illustrates a block diagram of an embodiment of the power supply circuit VG. The power supply circuit VG is formed of a voltage step-down power supply circuit for active condition and a voltage step-down power supply circuit for standby condition. The voltage step-down power supply circuits for active and standby conditions receive an external power supply voltage  $V_{ext}$  supplied to a semiconductor integrated circuit device LSI and form an internal voltage  $V_{int}$  supplied to the CPU and an internal circuit including a non-volatile storage element.

The voltage step-down power supply circuit for active condition amplifies the current to form the internal voltage  $V_{int}$  with a band-gap type fixed voltage generating circuit, a reference voltage 1 generating circuit to form the reference voltage  $V_{REF1}$  by switching of the trimming switch for a voltage dividing ratio of resistance with a trimming switch 1 setting signal, and an output buffer B1 consisting of a voltage follower type amplifying circuit to receive such reference voltage  $V_{REF1}$ . Namely, the band-gap type fixed voltage

generating circuit generates a temperature-compensated fixed voltage BGR1. The reference voltage 1 generating circuit amplifies the fixed voltage BGR1 up to the reference voltage VREF1 in the range, for example, of 1.4V to 1.6V required for the active condition by adjusting a voltage gain of the amplifying circuit A1 through the switching of the switch 1 for the voltage dividing ratio of resistance with the trimming switch 1 setting signal. Each circuit forming the voltage step-down power supply circuit for active condition is selectively activated with a control signal (enable 1) generated from the CPU.

The voltage step-down power supply circuit for standby condition forms the internal voltage Vint, for setting the predetermined step-down voltage while the power consumption is reduced, by amplifying the current with the reference voltage 2 generating circuit to form the reference voltage VREF2 by switching of the trimming switch for the connection of MOSFET in the threshold voltage difference type reference voltage generating circuit of the MOSFET with the trimming switch 2 setting signal and the output buffer B2 consisting of the voltage follower type amplifying circuit to receive such reference voltage VREF2. This reference voltage 2 generating circuit generates the reference voltage VREF2, for example, such as 1.3V to 1.7V which is required in the standby condition by switching of the

switch 2 for the connection of the MOSFET with the trimming switch 2 setting signal. The reference voltage 2 generating circuit and output buffer B2 forming the voltage step-down power supply circuit for active condition is selectively activated with the control signals enVREF2 and enOUT2.

When the internal circuit (Vint operating circuit) of the semiconductor integrated circuit device LSI is in the active condition, each circuit of the voltage step-down power supply circuit for active condition is activated with the control signal (enable 1). In this case, the output buffer 2 of the voltage step-down supply circuit for standby condition is non-activated with the control signal enOUT2. Accordingly, the internal circuit (Vint operating circuit) is operated with the internal voltage Vint formed with the voltage step-down power supply circuit for active condition. The reference voltage 2 generating circuit of the voltage step-down power supply circuit for standby condition may be non-activated like the output buffer B2 with the control signal enVREF2 but the reference voltage 2 generating circuit may be fixed to the active condition because the current flowing through the reference voltage 2 generating circuit itself is as small as can be neglected in comparison with the current consumed in the entire circuits of the semiconductor integrated circuit device in the active condition. Moreover, when

such current is fixed to the active condition, it will results in the merit that the switching time to the standby condition from the active condition can be reduced. Therefore, the control signal enVREF2 is fixed to the active level or it may be eliminated.

When the internal circuit (Vint operating circuit) of the semiconductor integrated circuit device is switched to the standby condition, each circuit of the voltage step-down power supply circuit for active condition is non-activated with the control signal (enable 1). Namely, a DC current is stopped to flow into the fixed voltage generating circuit forming the voltage step-down power supply circuit for active condition and the amplifying circuit A1 and trimming resistance of the reference voltage 1 generating circuit and the output buffer B1. The output buffer 2 is activated with the control signal enOUT2 and the internal voltage Vint corresponding to the reference voltage VREF2 formed by the reference voltage 2 generating circuit of the voltage step-down power supply circuit for standby condition is supplied to the internal circuit (Vint operating circuit). In the standby condition of the internal circuit, almost all operations of the internal circuits in the AC operation are stopped due to the stop of supply of the clock and the holding current of DC mainly flows.

Since operations of the internal circuit are

stopped, the current consumed in this period becomes a leak current flowing into the MOSFET or the like and the internal circuit holds the storing condition of the storage circuit such as a register and a latch circuit with the voltage step-down power supply circuit for standby condition. Accordingly, the current consumed in the semiconductor integrated circuit device LSI in the standby condition becomes the current consumed in the voltage step-down power supply circuit for standby condition and the leak current flowing into the internal circuit. Therefore, current consumption in the standby condition can be reduced up to about 1  $\mu$ A by lowering the current consumed in the voltage step-down power supply circuit for standby condition which will be described later.

Fig. 3 is a block diagram of another embodiment of the power supply circuit VG of Fig. 1. In this embodiment, operations of all circuits of the voltage step-down power supply circuit for active condition including the fixed voltage generating circuit are stopped to reduce power consumption in the standby condition. Therefore, a longer time is required until the operation of the voltage step-down power supply circuit for active condition is stabilized when the standby condition is switched to the active condition. When the internal circuit such as the CPU or the like operates before the operation of the voltage step-down

power supply circuit for active condition is stabilized, the internal voltage  $V_{int}$  is remarkably reduced due to the shortage of current supplied from the voltage step-down power supply circuit for active condition and thereby erroneous operation may be generated.

In this embodiment, a voltage detecting circuit consisting of a comparator CMP and a logic circuit is provided in the voltage step-down power supply circuit for active condition. The comparator CMP receives, at the reversed input (negative), the fixed voltage BGR1 formed in the fixed voltage generating circuit and also receives, at the non-reversed input (positive), the predetermined divided voltage of the voltage dividing resistance. The divided voltage is selected at the potential which is higher than the fixed voltage BGR1 under the condition that the reference voltage 1 generating circuit is in the stabilized operation.

Accordingly, since the fixed voltage BGR1 is higher than the divided voltage in the initial condition that the voltage step-down power supply circuit for active condition is activated with the control signal (enable 1), the comparator CMP forms the output signal of low level. When the reference voltage 1 generating circuit is almost stabilized in operation, the divided voltage becomes higher than the fixed voltage BGR1 and the comparator CMP forms the output signal of high level. The logic circuit delays this output signal to generate

the control signal READYREG.

The control signal READYREG is used as the control signal of a gate circuit G1 of the clock control circuit provided in the internal circuit. With the control signal READYREG, the gate circuit G1 opens the gate and supplies the clock CLK to the CPU. Accordingly, the CPU is once set to the active condition with the control signal (enable 1) and operates by receiving the supply of the clock CPUCLK corresponding to the control signal READYREG formed by delaying the output signal of the comparator which has changed to the high level. Thereby, erroneous operation as described above can be prevented.

Fig. 4 is a waveform diagram for describing an example of operations of the power supply circuit in relation to the present invention. In this figure, the signal waveforms under the condition that the standby condition is switched to the active condition and this active condition is switched again to the standby condition are illustrated. First, the control signal (enable 1) to drive the voltage step-down power supply circuit for active condition rises. Thereby, each circuit of the voltage step-down power supply circuit for active condition is activated and the fixed voltage BGR1 and the reference voltage VREF1 rise sequentially in this order.

Initially, the internal voltage Vint is held with the output buffer B1 for standby condition. During the

period where the standby condition is switched to the active condition, the output buffer B1 for active condition and the output buffer B2 for standby condition are operating simultaneously. Since the buffers having higher supply capability in the PMOS side are used for the two buffers, the output buffer B2 for standby condition in the higher voltage holds the internal voltage  $V_{int}$ . Accordingly, voltage drop due to collision of output voltages does not occur. As the reference voltage  $V_{REF1}$  rises, an output voltage from the output buffer B1 for active condition rises but since the internal voltage  $V_{int}$  is held to the higher level with the output buffer for standby condition under the condition that a load current is rather light, change of the internal voltage  $V_{int}$  cannot be seen initially.

The comparator CMP judges rise of the reference voltage  $V_{REF1}$  by dividing the reference voltage  $V_{REF1}$  and then comparing, under the normal condition, the divided voltage  $chkV_{REF1}$  which is a little higher than the fixed voltage  $BGR1$  with the fixed voltage  $BGR1$  and sets the control signal  $READYREG$  to the high level (logic 1) with the logic circuit. Thereby, the gate G1 of the clock control circuit opens, the supply of clock  $CPUCLK$  to the CPU can be started, the control signal  $enOUT$  supplied to the output buffer B2 of the voltage step-down power supply circuit for standby condition is changed to the low level, and the output buffer B2 is set to



the non-active condition. Accordingly, the internal voltage  $V_{INT}$  ( $=V_{int}$ ) under the active condition is set to the voltage ( $V_{INT} = V_{REF1}$ ) corresponding to the reference voltage  $V_{REF1}$ .

Even in the active condition as described above, the control signal  $en_{REF2}$  is set in the high level (always enable condition) and the reference voltage 2 generating circuit maintains the activated condition. Therefore, the reference voltage 2 generating circuit forms the reference voltage  $V_{REF2}$  but since the output buffer B2 is in the non-active condition (output high impedance condition), the internal voltage  $V_{INT}$  corresponds to the reference voltage  $V_{REF1}$ .

Switching to the standby condition from the active condition is instructed, although not particularly restricted, with the CPU and the control signal (enable 1) rises in this timing. Accordingly, each circuit of the voltage step-down power supply circuit for active condition is non-activated and thereby the  $READY_{REG}$  signal generating circuit consisting of the comparator CMP and logic circuit sets the control signal  $READY_{REG}$  to the low level (logic 0). Thereby, the gate G1 of the clock control circuit closes to stop the clock  $CPU_{CLK}$  for the CPU and set the CPU to the standby or sleeping condition. Moreover, it is more preferable that the control signal  $en_{OUT}$  is set to high level before the control signal (enable 1) and thereby the output buffer

B2 is activated. Accordingly, the internal voltage VINT (= Vint) under the standby condition is set to the voltage (VINT = VREF2) corresponding to the reference voltage VREF2.

Switching to the active condition from the standby condition is realized by raising the control signal (enable 1) by inputting an interruption signal to the CPU or by setting first only a timer circuit in the CPU to the operating condition and then raising, after passage of the constant period, the control signal (enable 1). Moreover, it is also possible to raise the control signal (enable 1) with an external signal.

Fig. 5 is a waveform diagram for describing an example of operations of the READYREG signal generating circuit of Fig. 3. The voltage chkVREF1 is a divided voltage of the reference voltage VREF1 and is selected, in the normal condition, to the voltage which is higher than the fixed voltage BGR1. Accordingly, immediately after the control signal (enable 1) described above has changed to the high level, the BGR1 is higher than the chkVREF1 ( $BGR1 > chkVREF1$ ). But, when operation is almost stabilized due to the amplifying operation in the reference voltage 1 generating circuit, above relationship is inverted ( $BGR1 < chkVREF1$ ). The comparator detects this condition and then changes the output signal to the high level from the low level. This output signal is delayed with the logic and the control

signal ERADYREG is then changed to the high level from the low level.

Fig. 6 is a block diagram of another embodiment of the power supply circuit VG of Fig. 1. In this embodiment, the semiconductor integrated circuit device itself includes the voltage step-down power supply circuit for standby condition performs the automatic trimming adjustment. In this embodiment, as the operation condition of the semiconductor integrated circuit device, the mode of "trimming of reference voltage for active/standby condition" is also provided in addition to the switching of the active/standby condition. Accordingly, the output buffer B4 for monitoring the reference voltage VREF2 and voltage selector SEL and comparator CMP are added.

Although not particularly restricted, a voltage to be set is impressed from an external terminal to the reversed input (negative) of the comparator CMP, while the reference internal voltage Vint having passed the selector SEL or a monitor voltage MON1 of the output buffer B4 is impressed to the non-reversed input (positive). The output buffer B4 is selectively activated with the control signal enMON1 which is provided in separation from the output buffer B2.

For example, in order to set the internal voltage Vint to 1.4 to 1.6V in the active condition and to 1.3 to 1.7V in the standby condition, the center voltage

of these voltages 1.5V is supplied to the external terminal. In the trimming mode of the reference voltage for active condition, the CPU raises the control signal (enable 1) to set the semiconductor integrated circuit device to the active condition, selects the internal voltage Vint corresponding to the reference voltage VREF1 with the selector SEL, and supplies this internal voltage Vint to the comparator CMP as the input signal CMPin. The comparator CMP compares this input signal with the reference voltage such as 1.5V and transfers the comparison result CMPout to the internal circuit such as the CPU or the like.

For example, as the trimming sequence, a voltage dividing ratio of the reference voltage 1 generating circuit is set to the minimum value and the switch 1 is then changed over to sequentially increase the voltage gain. When the reference voltage VREF1 is sequentially increased with the switching of the switch 1 and the comparison result CMPout of the comparator CMP has changed to the high level from the low level or when just preceding trimming switch 1 setting signal, namely the internal voltage Vint becomes nearest to 1.5V, the trimming switch 1 setting signal is detected and it is then stored in the non-volatile storage element. Thereafter, the trimming switch 1 setting signal stored in the non-volatile storage element is stored in a resistor or the like in order to form the control signal

of the switch 1.

In the trimming mode of the reference voltage for standby condition, the control signal (enable 1) is kept raised with the CPU, unlike the standby condition described above, to continuously set the semiconductor integrated circuit device in the active condition. Accordingly, the output buffer B4 is activated with the control signal enMON1. Namely, in the standby condition as described above, operations of the internal circuit is stopped and the operations in the trimming mode for the active condition can no longer be executed.

In this embodiment, since the control signal (enable 1) is kept raised to set the semiconductor integrated circuit device in the active condition, the internal voltage MON1 corresponding to the reference voltage VREF2 is selected with the selector SEL and it may be supplied as the input signal CMPin of the comparator CMP. This comparator CMP compares the reference voltage CMPbase such as 1.5V and transfers the comparison result CMPout to the internal circuit such as the CMP or the like.

As the trimming sequence in the standby condition, like that in the active condition, an output voltage of the reference voltage 2 generating circuit is set to the minimum value, the reference voltage VREF2 is sequentially raised through the switching of the switch 2, when the comparison result CMPout of the comparator

CMP is changed to the high level from the low level or when the just preceding trimming switch 2 setting signal, namely the internal voltage MON1 becomes nearest to 1.5V, the combination of the trimming switch 2 setting signal is detected and it is then stored in the non-volatile storage element. Thereafter, the control signal of the switch 2 can be formed by previously storing the trimming switch 2 setting signal stored in the non-volatile storage element to a register or the like.

In this structure, the time occupied with single tester can be reduced in order to reduce the cost required for testing by increasing the number of simultaneous measuring circuits per tester. Namely, a plurality of semiconductor integrated circuit device are connected in parallel to the tester and the reference voltage CMPbase is supplied thereto. Accordingly the trimming of a plurality of semiconductor integrated circuit devices can be performed simultaneously in parallel during the testing operation.

The comparator CMP for comparing the signal MON1 of the monitor terminal with the reference voltage (CMPbase) and the circuit for determining the new trimming data by judging the comparison result of the comparator CMP may be realized with an exclusive circuit which is formed of a random logic or the like in addition to the CPU. The trimming data can also be written into the non-volatile storage element with the similar signal

route. This non-volatile element can use the circuit included in the power supply circuit VG or the non-volatile storage circuit mounted to the semiconductor integrated circuit device LSI.

Fig. 7 illustrates a practical circuit diagram of an embodiment of the reference voltage 2 generating circuit of Fig. 2. In this embodiment, the control signal enVREF2 in the embodiment of Fig. 2 or the like is eliminated. This embodiment forms the constant voltage  $2 \times V_{TH}$  corresponding to the threshold voltage  $V_{TH}$  by applying the constant current to the diode-connected MOSFETM1 and M2. This constant voltage  $2 \times V_{TH}$  is outputted from a source follower circuit consisting of the MOSFETM3, M4 and the constant current sources provided to the sources thereof and the output voltage is then amplified with the amplifying circuit A2 to form the reference voltage VREF2.

A serial circuit of the MOSFETM1 and M2 is formed, as illustrated in the detail diagram, in the structure that a plurality of serial circuits consisting of a couple of diode-connected MOSFETs and a switch are provided in parallel. The switch described above is selectively turned ON with a trimming signal. Namely, a serial circuit including the switch in the ON state are connected in parallel. The MOSFETM1 and M2 typically indicate the MOSFETs connected in parallel with the switch.

The MOSFETM1 and M2, forming the serial circuit described above are given the threshold value which is larger than that of the MOSFETM3 to M6 forming the source follower circuit or the like. Although not particularly restricted, the MOSFETM1, M2 is caused to have the threshold voltage  $V_{TH1}$  which is larger than the threshold voltage  $V_{TH2}$  of the MOSFETM3 or the like to which the ion is not implanted because the ion is implanted to the channel area thereof in order to make higher the impurity concentration. Accordingly, the voltage of node N1 in the MOSFETM1 and M2 is set equal to the voltage  $2 \times V_{TH1}$ . Since this voltage  $2 \times V_{TH1}$  is outputted via the gate and source of the MOSFETM3, M4, the voltage of node N2 is set equal to  $2 \times V_{TH1} - 2 \times V_{TH2}$ .

As described above, the threshold voltage  $V_{TH}$  is used as the reference voltage of the difference voltages of the gate and source voltages  $V_{GS}$  of different two kinds of MOSs. In this embodiment, a current value of the constant current source 11 which applies a current to the MOSFET to reduce power consumption is set, for example, to the value as low as 100 nA. A bias current of the amplifying circuit A1 is also set to 100 nA. The current flowing into the MOSFETM5, M6 to set the gain of the amplifying circuit A1 is set to about 200 nA. Accordingly, current consumption of the reference voltage 2 generating circuit is controlled to about 500



nA.

The MOSFETM1 and M2 are set depending on the number of MOSFETs connected in parallel as described above. Namely, when the total width of the MOSFETs connected in parallel is increased to N, the current of 100 nA formed by the constant current source I1 is distributed corresponding to the number of parallel connections and the current flowing into one serial circuit is reduced to  $1/N$ . Therefore, since the current per unit width of the MOSFETs represented by M1 and M2 is reduced, the gate and source voltage  $V_{GS}$  ( $V_{TH1}$ ) is reduced to lower the voltage  $2 \times V_{TH1}$ . Accordingly, the voltage ( $2 \times V_{TH1} - 2 \times V_{TH2}$ ) of the node N2 is also lowered. Since this voltage is then amplified up to two times the voltage of the amplifying circuit A2 ( $M5 = M6$ ), the reference voltage  $V_{REF2}$  can be adjusted.

This trimming method is essentially based on the adjustment of current density. In the figure, the current is expressed as the equal current I1 but this trimming is also possible by varying the current of the current source of the MOSFETM1, M2 and the current of the current source of the MOSFETM3, M4. In this circuit, the type of MOS (particularly, the gate width W, gate length  $L_g$  and allocation) is identical in the MOSFETM1, M3, M3 and when the current is totally equal to I1, difference of devices can be canceled, resulting in the merit that the reference voltage can be controlled only

with difference of implantation of the MOSFETM1, M2, M3.

When the width of MOSFETM1, M2 is changed to N-times with the trimming,  $V_{REF2}$  can be expressed as  $2 \times 2 \times (V_{TH1} - V_{TH2} - S \times \log_{10}(N))$  in order to operate, for example, MOS in the sub-threshold region. Here, S is the sub-threshold swing [V/10 times]. From this formula, it can be understood that voltage can be adjusted with the trimming and the influence of temperature characteristic of sub-threshold swing S is intensified as the voltage is more deviated from the condition,  $N=1$ .

Fig. 8 illustrates a practical circuit diagram of another embodiment of the reference voltage generating circuit of Fig. 2. Even in this embodiment, the control signal  $enV_{REF2}$  in the embodiment of Fig. 2 is also eliminated. In this embodiment, temperature compensation can be realized as well as the voltage trimming. In this embodiment, the forward voltage in the forward bias of the PN-junction diode D1 is transferred with a voltage follower circuit of the multiple stage connection. The voltage of each stage is selected with the selector SEL to be controlled with the trimming setting signal and it is then transferred to the output buffer B2.

In this embodiment, the differential amplifying circuits A11 to A1N forming the voltage follower circuit are respectively formed to provide different widths such

as 1:M to the differential MOSFETQ1 and Q2 as represented by the differential amplifying circuit A11. A current Miller type N-channel load MOSFET provided in the drain side of these differential MOSFETQ1 and Q2 is set to 1:1 in size and controlled to apply the equal current to the differential MOSFETQ1 and Q2. Accordingly, a current density difference is generated in the differential MOSFETQ1 and Q2 and thereby an offset voltage is generated in proportional to the sub-threshold swing S.

Whenever the forward voltage in the forward bias of the diode D1 passes the single stage of the voltage follower circuits A11 to A1N of the multiple stage structure, an offset voltage is accumulated. Therefore, the reference voltage VREF2 of the desired voltage value and temperature characteristic can be extracted by obtaining an output of the desirable number of stages with the selector SEL. Even in this embodiment, for the purpose of low power consumption, a current value of the diode D1 and the constant current source I<sub>o</sub> provided to the differential amplifying circuits A11 to A1N is set as low as about 50 nA. Accordingly, even when the differential amplifying circuits are provided in many stages, power consumption can be lowered as in the case of Fig. 7.

In this embodiment, since MOSFET is used to form the reference voltage VREF2 which allows the trimming,

the area to be occupied with the voltage step-down power supply circuit for standby condition can be reduced. For instance, when the voltage step-down power supply circuit for standby condition is formed with a resistance trimming circuit like the voltage step-down power supply circuit for active condition, a resistance value as high as  $15\text{ M}\Omega$  is required for the purpose that only the current as low as about  $100\text{ nA}$  is applied by setting the reference voltage  $V_{REF2}$  to  $1.5\text{V}$  to realize low power consumption. In view of realizing such high resistance element with a polysilicon resistance element, the occupation area as wide as that required to mount about 50 MOSFETs will be required.

Fig. 9 illustrates the temperature characteristic diagram for describing operations of the reference voltage 2 generating circuit of Fig. 8. Since the forward voltage of the PN junction diode D1 has the negative temperature characteristic as is well known, while the sub-threshold swing S has the positive temperature characteristic, as the a larger number of offset voltages are added as the number of taps increases, the temperature characteristic changes to the positive characteristic from the negative characteristic. In the temperature characteristic of Fig. 8, only one characteristic is selected from the characteristic tap00 to tap07 corresponding to a plurality of selection taps considering the operation environment temperature

of the semiconductor integrated circuit device. When the priority is given to the temperature characteristic, the characteristic tap03 and the characteristic tap04 are selected. When the voltage range of the reference voltage VREF2 is in the allowable range, a certain dependence on temperature may be left to obtain the desired voltage.

Fig. 10 illustrates a circuit diagram of another embodiment of the voltage step-down power supply circuit for active condition. In this embodiment, the fixed voltage BGR1ub formed in the fixed voltage generating circuit is indicated as the value which is higher than the reference voltage VREF1. The fixed voltage BGR1ub formed in the fixed voltage generating circuit is current-amplified with the buffer circuit B5 consisting of the voltage follower circuit up to the fixed voltage BGR1. This fixed voltage BGR1 is divided with a voltage dividing resistance circuit and the voltage at each voltage dividing point is selected with the switch 1 which is controlled with the trimming switch 1 setting signal. The divided voltage VREF1ub selected with the switch 1 is current-amplified with the buffer circuit B6 consisting of the voltage follower circuit up to the reference voltage VREF1 and is then outputted as the internal voltage Vint through the output buffer B1.

In this embodiment, since the fixed voltage BGR1 is divided to form the reference voltage VREF1 as

described above, the reference voltage  $V_{REF1}$  is supplied as the voltage  $tat$  to the non-reversed input (positive) of the comparator  $CMP$  of the  $READYREG$  generating circuit, while a divided voltage  $chk$  which is lower than the divided voltage for the trimming is supplied to the reversed input (negative).

The control signal (enable 1) of the voltage step-down power supply circuit for active condition is supplied, as a start signal ( $compstart$ ) to the delay circuit  $TD1$ , gate circuit  $G2$  and gate circuit  $G3$ . With the high level of the signal delayed with the delay circuit  $TD1$  and the high level of the output signal of comparator  $CMP$ , an output signal of the gate circuit  $G2$  is set to the high level, and this output signal is delayed again with the delay circuit  $TD2$  to output the  $READYREG$  signal through the gate circuit  $G3$  which opens the gate with the control signal (enable 1). The reference voltage  $chk$  of the comparator  $CMP$  rises quicker than a comparison voltage ( $tgt$ ) but since this signal is raised with the control signal (enable 1 ( $compstart$ )) and the comparator  $CMP$  itself is activated from the non-active condition, comparison result in the delay time  $td1$  period immediately after the start signal ( $compstart$ ) becomes unstable. Therefore, the comparator output is masked by defining the delay time  $TD1$  as the unstable period. In this embodiment, the time up to unstable operation when the reference voltage

1 generating circuit is started is attained with the time setting of the delay circuits TD1, TD2 described above. The comparator CMP is mainly provided to verify operations of the buffer circuit B6.

Fig. 11 illustrates a circuit diagram of another embodiment of the READYREG signal generating circuit provided to the voltage step-down power supply circuit for active condition. The voltage step-down power supply circuit for active condition is similar to the embodiment of Fig. 2. In this embodiment, the voltage chkVREF2 which is lower than the normal value of chkVREF1 obtained by adequately dividing the reference voltage VREF2 is used for determination of rise of the reference voltage VREF1. Namely, since the reference voltage 2 generating circuit of the voltage step-down circuit for standby condition steadily forms the reference voltage VREF2, the voltage chkVREF2 obtained by dividing such reference voltage steadily maintains the constant voltage level even in the standby condition and active condition.

Accordingly, since the voltage step-down power supply circuit for active condition is activated with the control signal (enable 1) and the comparator detects that the divided voltage chkVREF1 exceeds the voltage chkVREF2, rise of the VREF2 can be determined as illustrated in Fig. 3. The logic circuit for processing the output signal of the comparator CMP is similar to

that of Fig. 10. Namely, the comparator CMP compares the tgt voltage with the chk voltage which is a little lower than the final value, determines the tgt voltage has exceeded the final value, and thereafter outputs the READYREG signal after waiting for the assumed time TD2 where the voltage reaches the final value. The logic circuit is similar to that of Fig. 10.

Fig. 12 illustrates a block diagram of another embodiment of the power supply circuit VG of Fig. 1. In this embodiment, a power supply for testing a DC current (iddq) of the semiconductor integrated circuit device is provided. In the iddq testing, a current flowing from an external terminal Vext of the semiconductor integrated circuit device is measured while the internal circuit is operated slowly to detect poor insulation of the elements and wirings.

The voltage step-down power supply circuit for active condition is required to have comparatively large current supplying capability in order to obtain stable internal voltage Vint even when the internal circuit is operated in the high speed. Namely, it is required to have the large current supplying capability to provide stable internal voltage Vint even when the operation current consumed in the internal circuit and it is also required that a large current flows into the voltage step-down power supply circuit for active condition. Accordingly, the current flowing in the



voltage step-down power supply circuit for active condition becomes larger than the leak current generated by poor insulation in the iddq testing and thereby detection of leak current becomes difficult.

In order to solve this problem, a voltage step-down power supply circuit for iddq testing is also provided. This voltage step-down power supply circuit for iddq testing is formed of the output buffer B3 to simplify the circuit. Namely, the internal voltage  $V_{int}$  is formed by inputting the reference voltage  $V_{REF1}$  formed by the reference voltage 1 generating circuit to the output buffer B3. Therefore, the control signal (enable 2) for iddq testing is provided in addition to the control signal (enable 1) for active condition and these are used to activate the output buffer B3. The reference voltage 1 generating circuit is activated in the active condition and iddq testing with the control signal (enable) formed in the OR gate circuit G4 to receive the control signals (enable 1 and enable 2).

The output buffer B3 can set the operation current to a value which is lower than that of the output buffer B1 because the internal circuit operates slowly during the iddq testing. Accordingly, the current consumed by the voltage step-down power supply circuit can be reduced during the iddq testing and thereby detection accuracy of leak current generated due to poor insulation becomes high. If current consumption in the

aforementioned reference voltage 1 generating circuit cannot be neglected, it is also allowed that operation of the voltage step-down power supply circuit for active condition is stopped in the  $iddq$  testing mode and the internal voltage  $V_{int}$  is formed with the output buffer B3 using the reference voltage  $V_{REF2}$  of the reference voltage 2 generating circuit for standby condition.

Fig. 13 illustrates a circuit diagram of another embodiment of the READYREG generating circuit provided in the voltage step-down power supply circuit for active condition. In the amplifier (amplifying circuit) A1 of this embodiment, the output stage MOSFETMP 101 of the P channel is provided in the differential amplifying circuit and the gate  $V_{plimit}$  is connected, in the current Miller profile, to the P channel MOSMP 401 for current limitation of the output stage of the READYREG generating circuit. Therefore, the current flowing into a parasitic capacitance  $C_{REF1}$  to form the reference voltage  $V_{REF1}$  corresponds to the current flowing into the comparator CMP for comparing the fixed voltage  $BGR1$  with the divided voltage  $chkV_{REF1}$ . A delay capacitance  $CDLY2$  is also provided at the output of the comparator CMP.

The initial value in the standby condition is  $BGR1 = V_{REF1} = NDLY2 = READYREG = 0V$  (low level). When the control signal (enable 1) rises, the switch MOSFETMN 432 or the like which has determined the initial value

such as the RDYRESET signal turns OFF and the fixed voltage BGR1 of the fixed voltage generating circuit starts to rise. Subsequently, the MOSFETMP 101 of the amplifier A1 raises the reference voltage VREF1 while it is charging the capacitances CPH1 and CREF1. When the level of the divided voltage chkVREF1 of the reference voltage VREF1 exceeds the fixed voltage BGR1, an output of the comparator CMP is inverted, the P channel MOSFETMP 402 turns ON, and the NDLY2 signal starts to rise.

The current flowing into the node NDLY can be reduced to a small current determined with a Miller ratio (size ratio) because the MOSMP101 and MP401 which are supplying the current to the node VREF1 are Miller-connected via the Vplimit. When the NDLY2 signal exceeds the threshold of the inverters IV1, IV2, the READYREG signal becomes high level. Since the current to form the READYREG signal can be reduced to a small current, the delay capacitance CDL2 having small capacitance value (size) may be used.

When the active condition is changed to the standby condition, the RDYRESET2 signal is set to the high level to turn ON the MOSFETM 432 and set the READYREG signal to the low level. The RDYPRESET2 signal becomes low level to turn ON the P channel MOSFETMP 422 and forcibly sets the READYREG signal to the high level.

In the description of each embodiment, the part

not related to the present invention is eliminated. For example, considerations to prevent breakdown and to realize recovery for initial values before the trimming, throwing of the power switch and partial erroneous operation are required in any portion of the chip. Addition or deletion of signals for these portions in the circuit disclosed in the present invention is never inhibited.

The present invention has been described above practically based on the embodiments thereof. However, the present invention is never restricted thereto and allows various changes or modifications within the scope not departing from the claims thereof. For example, the fixed voltage generating circuit and the reference voltage 1 generating circuit can employ various embodiments because there is no limitation on the current consumption. The voltage step-down circuit for standby condition is enough when it can realize the trimming by utilizing the threshold voltage difference of the MOSFETs. The present invention can be applied to various digital signal processing circuits including a microprocessor or the like and also to the semiconductor storage device such as dynamic RAM and static RAM or the like including the active mode for the write and read operations and the standby mode for holding the stored information.

The typical inventions of the present invention

can provide the following effects. The semiconductor integrated circuit device which has realized high performance and low power consumption in a smaller area can be obtained by amplifying a fixed voltage formed in the fixed voltage generating circuit with an amplifying circuit which can adjust the voltage gain with a resistance circuit and a switch controlled with the first trimming switch setting signal, outputting an internal step-down voltage when the internal circuit is in the active condition with the first output buffer which is activated with the first control signal, forming the second reference voltage by adjusting combination of the threshold voltages with a plurality of MOSFETs and the switch controlled with the second trimming switch setting signal, and then outputting an internal step-down voltage when the internal circuit is in the standby condition with the second output buffer which is activated with the second control signal.